IN THE SPECIFICATION:

Please amend paragraph number **[0001]** as follows:

[0001] This application is a divisional of application Serial No. 09/917,127 filed July 27, 2001, ~~pending,~~ now U.S. Patent 6,780,746, issued August 24, 2004, which is a divisional of application Serial No. 09/586,243, filed June 2, 2000, ~~pending.~~ now U.S. Patent 6,717,245, issued April 6, 2004.

Please amend paragraph number **[0023]** as follows:

[0023] Semiconductor substrate 10 may comprise a wafer, as defined above, including a plurality of individual die locations thereon. The bond pads 12 are "bumped" with intermediate conductive elements 20 which project upwardly from active surface 14, or some or all of the ~~input\output~~ input/output locations for each die are redistributed using conductive traces prior to being bumped, such processes being well known in the art. If the external conductive elements (see below) are metallurgically incompatible with bond pads 12, the intermediate conductive elements 20 may be of a layer or layers of metals which will provide a better metallurgical bond therebetween. One such example, in the case of Al bond pads and tin/lead solder external conductive elements, would be to form intermediate conductive elements 20 of three superimposed layers (top to bottom) of copper, copper/chromium alloy, and chromium. It is also contemplated that the bond pads 12 may be bumped using a wire bonding capillary, or with solder of a higher melting temperature than that of another solder to be employed in external conductive elements 32, as referenced below. Intermediate conductive elements 20 may also comprise a conductive or conductor-filled epoxy, such as a silver-filled epoxy. The only significant constraints on the material and configuration selected for intermediate conductive elements 20 are compatibility with the bond pads 12 or other input/output contacts on substrate 10 as well as with external conductive elements 32, and sufficient temperature tolerance and physical strength to withstand encapsulation of active surface 14 of substrate 10 and formation of external conductive elements 32 thereon.

Please amend paragraph number **[0024]** as follows:

[0024] A preferred semiconductor substrate 10 has a standardized number of bond pads 12 or other input/output locations ~~12 for~~ for every die location (the term "bond pad" as used herein also encompassing redistributed input/output locations), the bond pads 12 being located in arrays, one array for each die location, with bond pads 12 laterally spaced from one another at, for example, a uniform pitch. The arrays are positioned at specific locations relative to a reference point (not shown) of the semiconductor substrate 10, in order to facilitate precise relative positioning of semiconductor substrate 10 and processing equipment therefor. This reference point may include the side edge of semiconductor substrate 10 or a center line of substrate 10 (not shown). Alternatively, the number, pitch and array configuration of bond pads 12 may be nonstandardized, for example, if different input/output arrangements are desired for dice formed on the same substrate 10.

Please amend paragraph number **[0025]** as follows:

[0025] After the formation of bond pads 12, FIG. 1B depicts how a plurality of channels or troughs 26 is formed on the active surface 14 of semiconductor substrate 10 to define individual die locations on substrate 10. As used herein, the term "individual dice" specifically includes, without limitation, partial wafers bearing more than one die as well as single dice. Channels or troughs 26 extend at a depth sufficient enough to pass entirely through the at least one layer 16 of integrated circuitry 18 upon the active surface 14 of substrate 10 and are cut in a grid pattern comprising a first group of mutually parallel channels or troughs 26 which are arranged perpendicular to a second group of mutually parallel channels or troughs 26. The channels or troughs 26 are located to extend along the so-called "streets" between individual semiconductor die locations on substrate 10, wherein neither active ~~or~~ nor passive components of integrated circuitry 18, or interconnect structures for same, are typically located. Various types of methods may be utilized to form channels or troughs 26 having different cross-sectional configurations. For example, a beveled or chamfered channel as shown may be formed using a wafer saw blade or an isotropic etch. A laser drill may be used to form a parallel-sided channel,

while an etching process, such as dry or plasma etching or wet solution etching, may be used to form channels with either substantially parallel sides or sloped sides, depending upon the anisotropic or isotropic tendencies of the etch employed. Each one of these types of cutting has advantages and disadvantages over the other types and it will be readily apparent to those skilled in the art which applications would be best used under particular circumstances. For example, where deep channels are preferred or required, wafer saw scribing is preferable as it is rapid and accurate. Where small-dimensioned channels with tolerances that must be tightly controlled are preferred or required, dry or wet etches would be utilized.

Please amend paragraph number **[0029]** as follows:

[0029] Once solder paste has been applied to bond pads 12, the solder paste is reflowed to form external conductive elements 32 in the form of substantially spherical ~~balls 32,~~ balls, as illustrated in FIG. 1E. The solder paste can be melted by any suitable means, such as electrical resistance or hot gas heating, forced air oven, radiant heating, liquid immersion, vapor phase condensation methods, or by any method of reflowing known in the art. Temperatures used to accomplish the reflowing of the solder paste are necessarily dependent on the composition of the solder paste being used. Heating times and temperatures must, therefore, be closely controlled to prevent melting or decomposition of the semiconductor substrate 10, including the substructures thereon (e.g., intermediate conductive elements 20, bond pads 12 and the underlying integrated circuitry 18). With these variables in mind, an appropriate solder paste must be selected for use in conjunction with a selected semiconductor substrate.

Please amend paragraph number **[0030]** as follows:

[0030] It is noted that any size of ~~ball~~ conductive element 32 may be formed so long as the dimensions of the ball comply with design constraints of the final semiconductor device. For most applications, ~~balls 32~~ conductive elements 32, in the form of balls, may have a diameter of from about 5 mil to about 15 mil. Because larger and smaller ball bond dimensions are envisioned for a variety of structures, other sized balls may be similarly manufactured.

Please amend paragraph number **[0033]** as follows:

[0033] FIG. 2 depicts how encapsulant material 30 may be applied to both the active surface 14 and the back side 22 of semiconductor substrate 10 in a substantially conformal manner so as to fill in channels or troughs 26, but not to overfill same to the point of being level with the top surfaces of intermediate conductive elements 20. The depressions 29 (shown in FIGS. ~~1B-1D~~ 1C-1E and 2 by broken lines) of the encapsulant material 30 over channels or troughs 26 are useful in that during the dicing operation, the recessed portions of encapsulant material 30 over channels or troughs 26 provide alignment guidance for the dicing of the substrate 10 into discrete semiconductor devices 34. Again, channels or troughs 26 extend below the layer 16 of integrated circuitry 18 on active surface 14 of semiconductor substrate 10. As is shown, the substrate 10 has been singulated into discrete semiconductor devices 34. The sloped ~~sidewalls~~ side walls of the encapsulant material 30 extend past the edges of layer 16 exposed by, for example, scribing with a wafer saw in such a manner as to provide a substantially hermetic seal against water, dust, and other contaminants that might otherwise damage or otherwise compromise the integrity and operation of semiconductor device 34. The intermediate conductive elements 20, if not completely ~~covered but~~ covered, being only partially ~~covered~~ covered, but supported at their peripheries by encapsulant material 30 as shown in broken line at 36, may in fact be used for connection to higher-level packaging without further disposition of external conductive elements 32 thereon and also without planarization, except to an extent necessary to ensure good exposure of the conductive materials of intermediate conductive elements 20. If completely covered, the upper ends of intermediate conductive elements 20 may be exposed by abrasive planarization, or the encapsulant material 30 selectively etched to expose the upper ends.